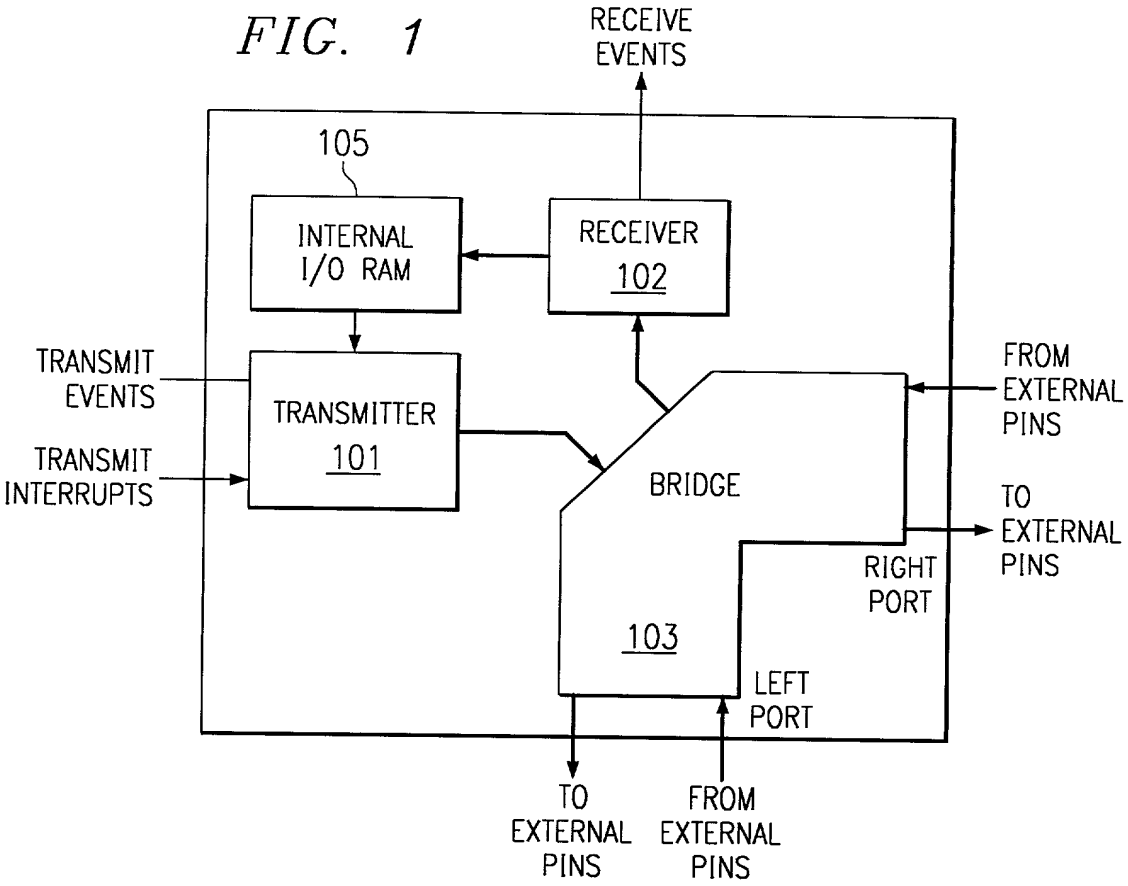
FIG. 1


RECEIVE EVENTS
105
INTERNAL I/O RAM
RECEIVER 102
TRANSMIT EVENTS
TRANSMIT INTERRUPTS
TRANSMITTER 101
BRIDGE
FROM EXTERNAL PINS
TO EXTERNAL PINS
RIGHT PORT
103
LEFT PORT
TO EXTERNAL PINS
FROM EXTERNAL PINS

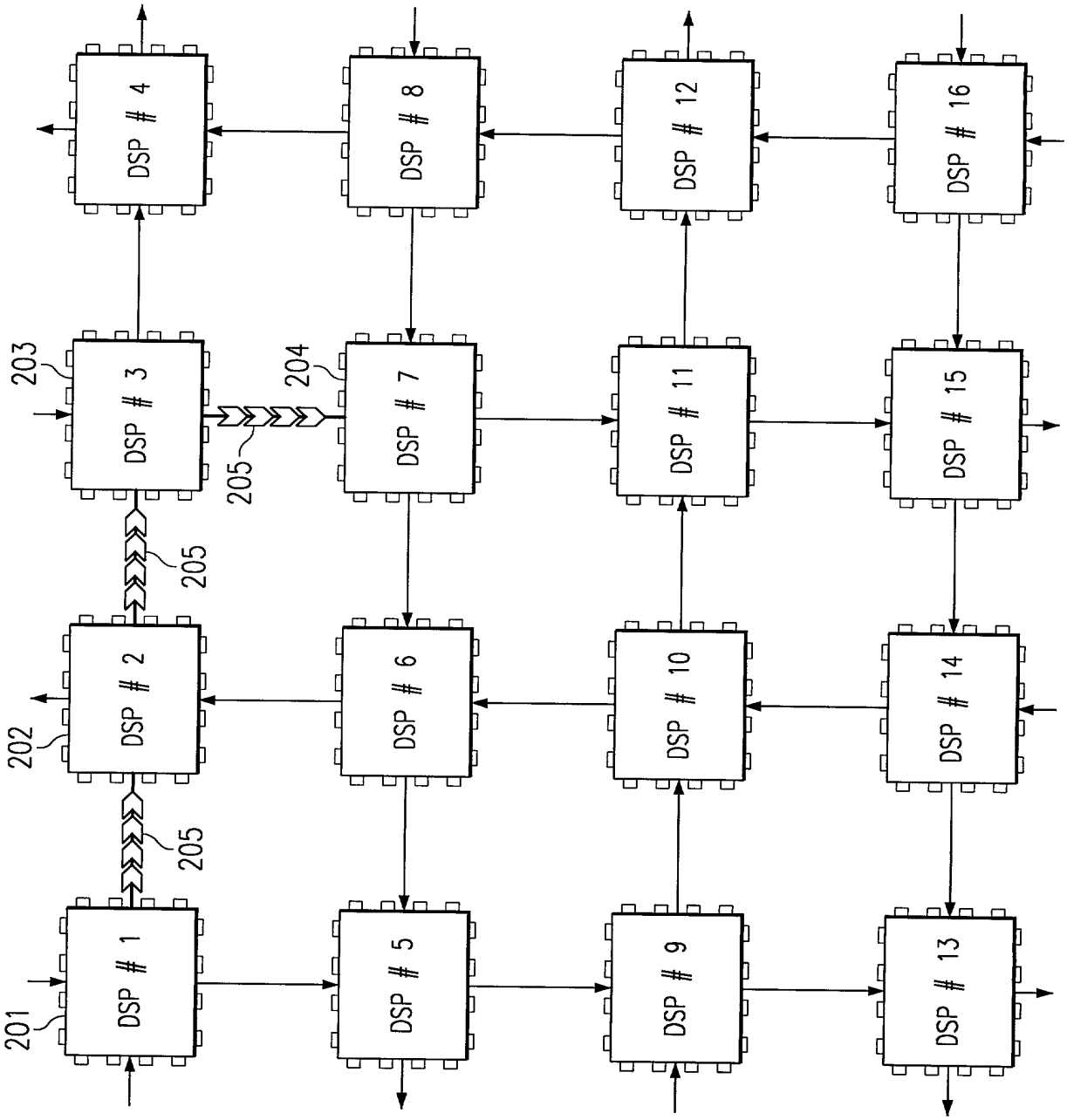

DSP # 1
DSP # 2
DSP # 3
DSP # 4
DSP # 5
DSP # 6
DSP # 7
DSP # 8
DSP # 9
DSP # 10
DSP # 11
DSP # 12
DSP # 13
DSP # 14
DSP # 15
DSP # 16
201
202
203
204
205
205
205

FIG. 2

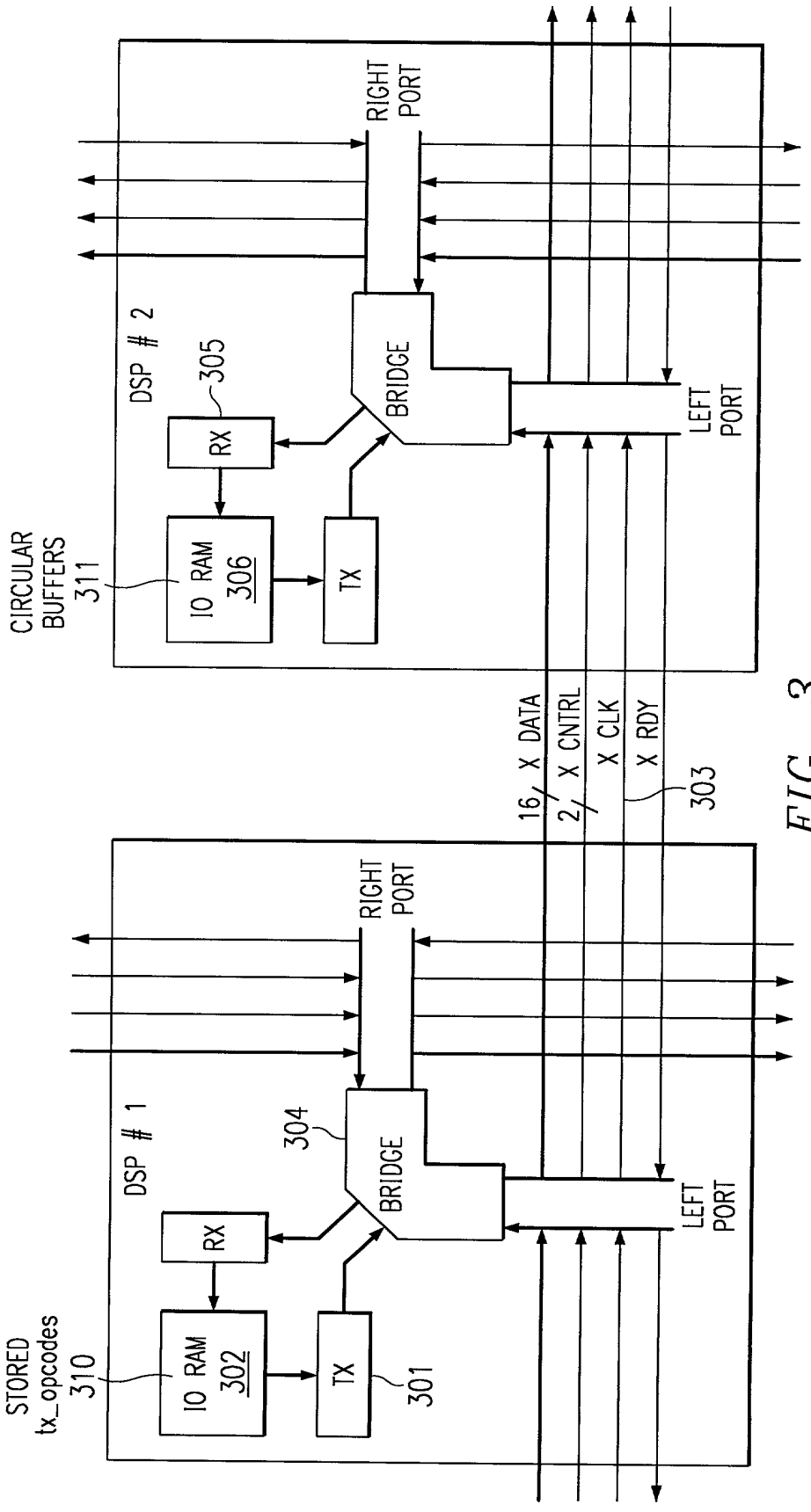

DSP # 1
DSP # 2
RIGHT PORT
LEFT PORT
BRIDGE
304
RX
TX
IO RAM 302
STORED tx_opcodes 310
301
IO RAM 306
CIRCULAR BUFFERS 311
305
16 X DATA
2 X CNTRL
X CLK
X RDY
303

FIG. 3

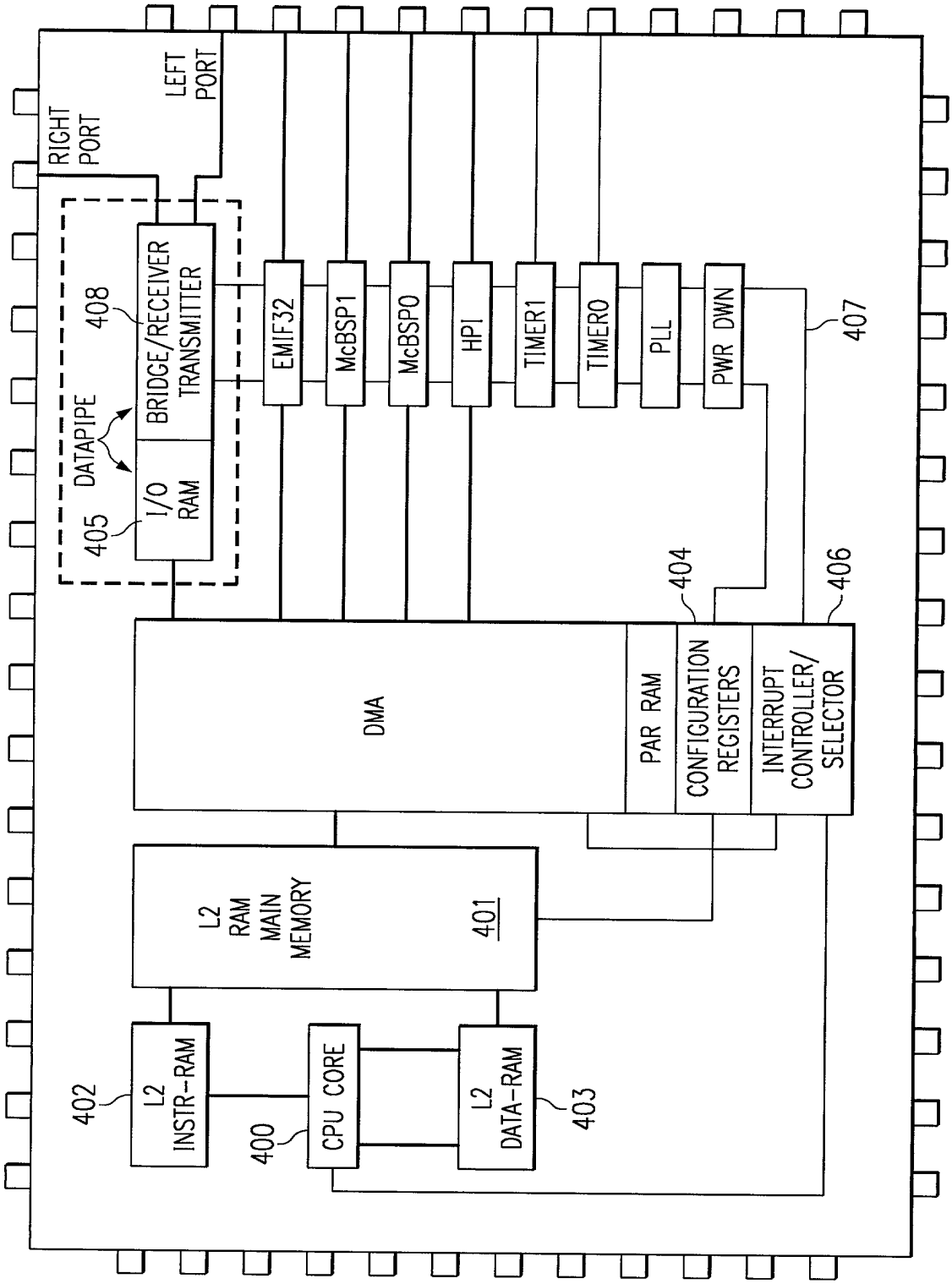

RIGHT PORT
LEFT PORT
DATAPIPE
408
BRIDGE/RECEIVER TRANSMITTER
I/O RAM
405
EMIF32
McBSP1
McBSP0
HPI
TIMER1
TIMER0
PLL
PWR DWN
407
DMA
404
PAR RAM
CONFIGURATION REGISTERS
INTERRUPT CONTROLLER/ SELECTOR
406
L2 RAM MAIN MEMORY
401
402
L2 INSTR-RAM
400
CPU CORE
L2 DATA-RAM
403

FIG. 4

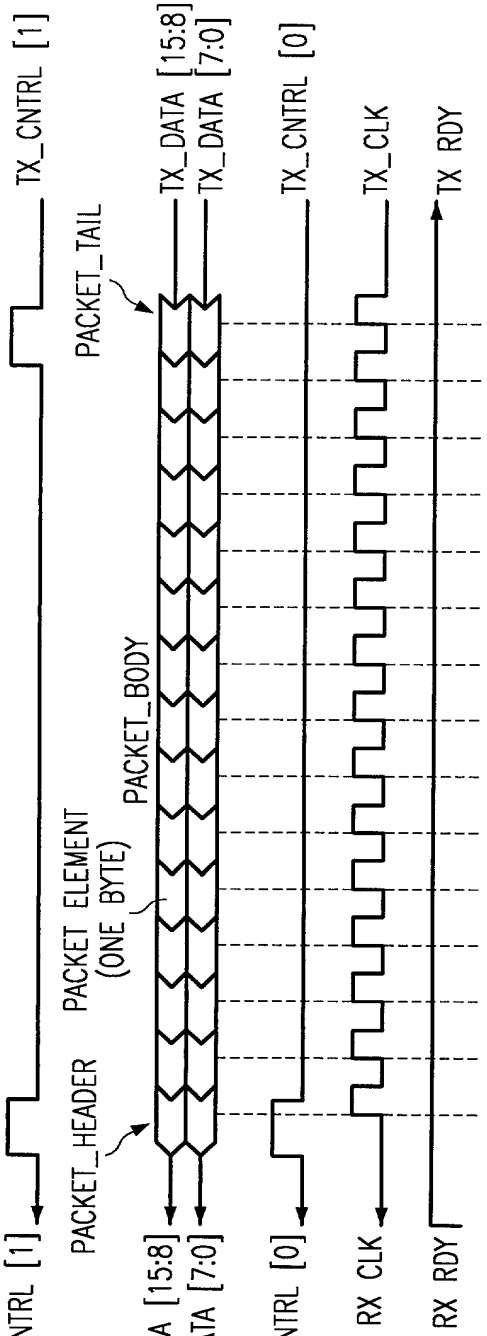

TX_CNTRL [1]
PACKET_TAIL
TX_DATA [15:8]
TX_DATA [7:0]
PACKET_BODY
PACKET ELEMENT (ONE BYTE)
PACKET_HEADER
TX_CNTRL [0]
TX_CLK
TX RDY
RX_CNTRL [1]
RX_DATA [15:8]
RX_DATA [7:0]
RX_CNTRL [0]
RX CLK
RX RDY

FIG. 5

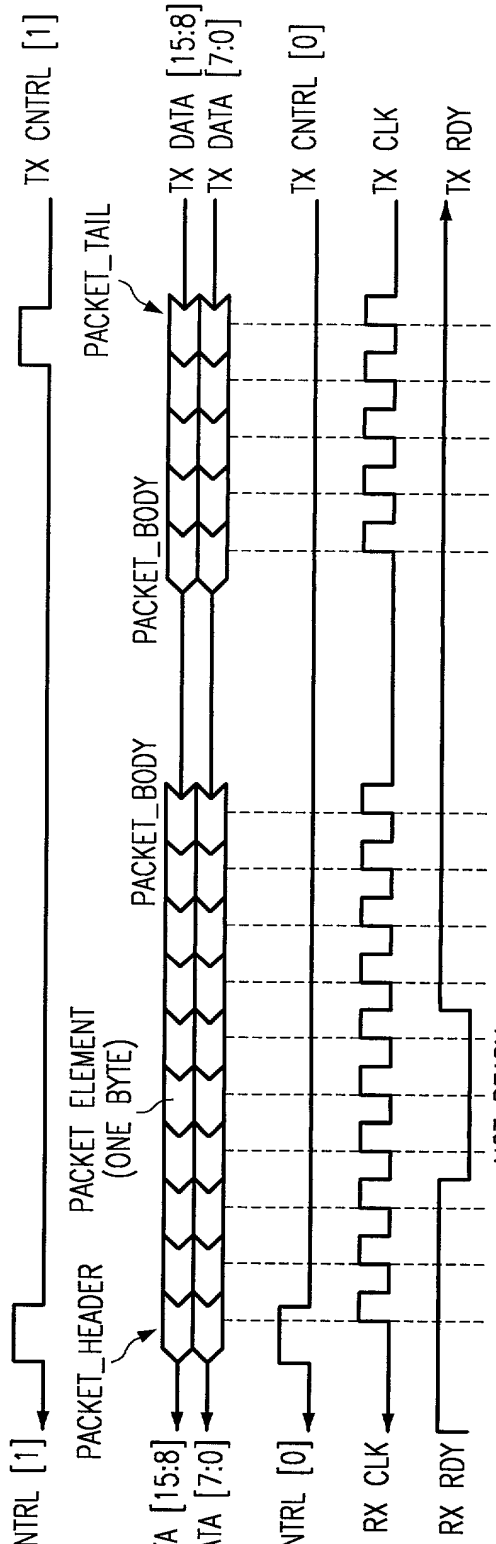

TX CNTRL [1]
PACKET_TAIL
TX DATA [15:8]
TX DATA [7:0]
PACKET_BODY
PACKET ELEMENT (ONE BYTE)
PACKET_HEADER
TX CNTRL [0]
TX CLK
TX RDY
NOT READY
RX CNTRL [1]
RX DATA [15:8]
RX DATA [7:0]
RX CNTRL [0]
RX CLK
RX RDY

FIG. 6

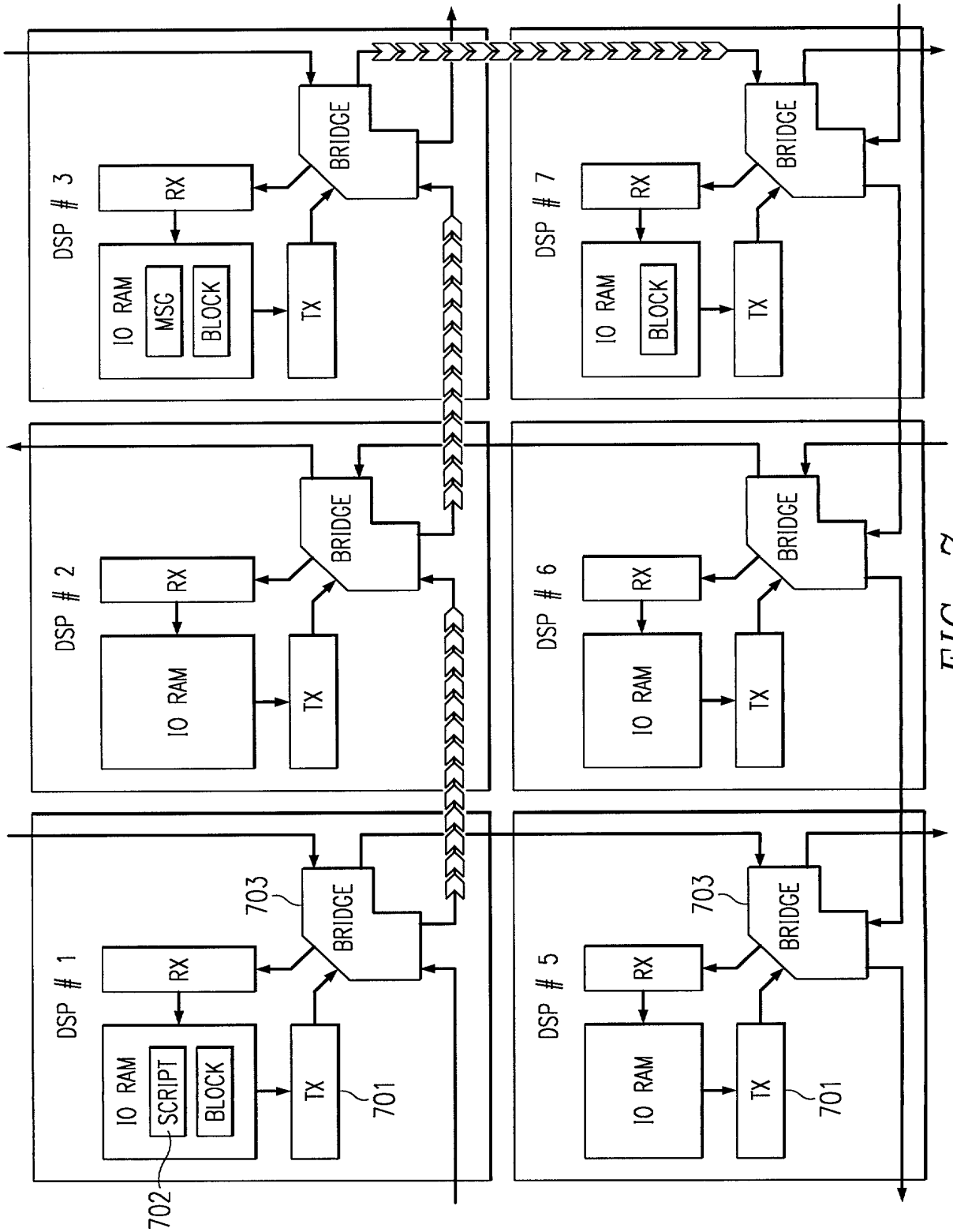

DSP # 1
IO RAM
SCRIPT
BLOCK
RX
TX
BRIDGE
703
701
702
DSP # 2
IO RAM
RX
TX
BRIDGE
DSP # 3
IO RAM
MSG
BLOCK
RX
TX
BRIDGE
DSP # 5
IO RAM
RX
TX
BRIDGE
703
701
DSP # 6
IO RAM
RX
TX
BRIDGE
DSP # 7
IO RAM
BLOCK
RX
TX
BRIDGE

FIG. 7

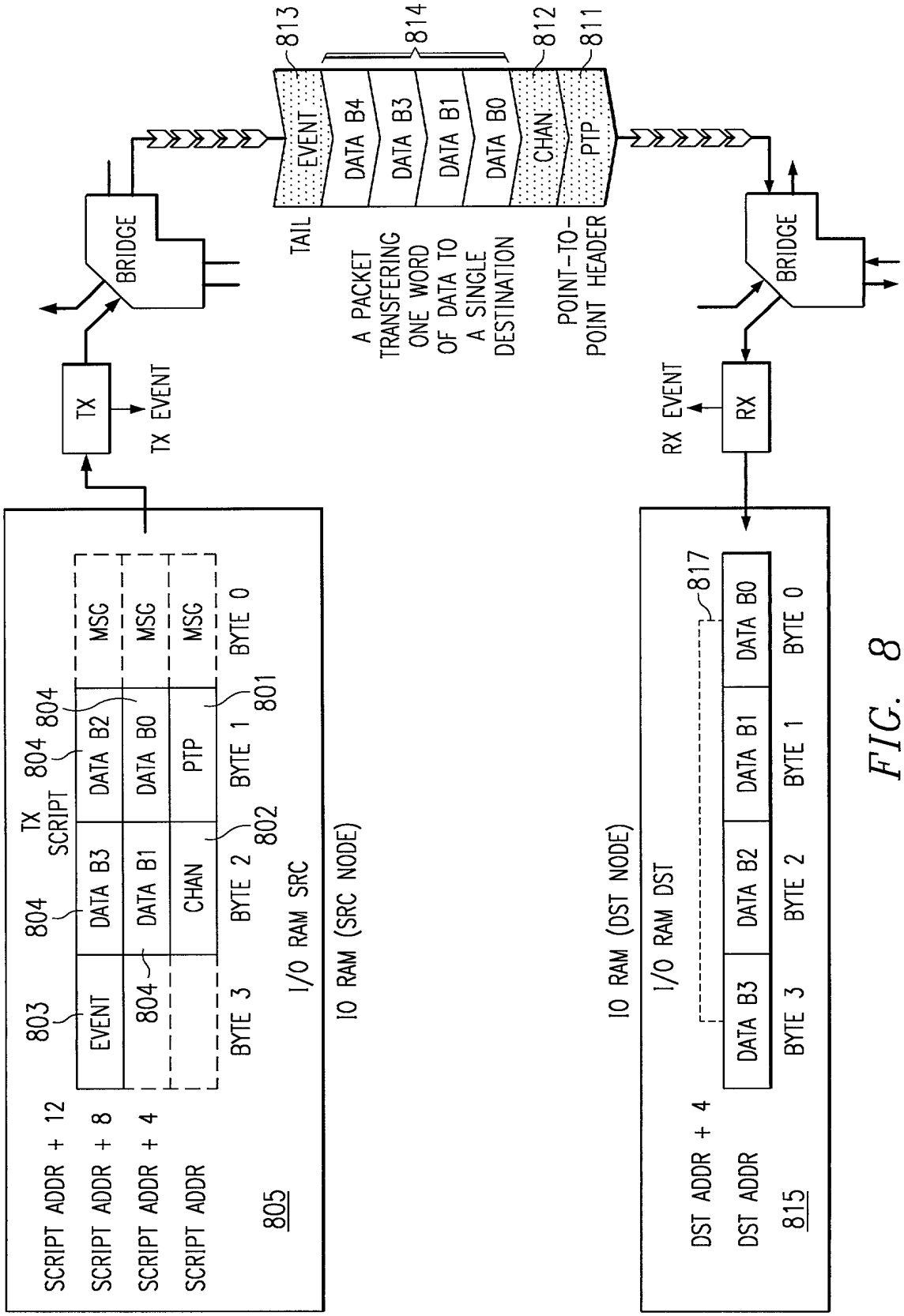

SCRIPT ADDR + 12
SCRIPT ADDR + 8
SCRIPT ADDR + 4
SCRIPT ADDR
805
803
804
EVENT
DATA B3
DATA B1
CHAN
BYTE 3
BYTE 2
TX SCRIPT
804
DATA B2
DATA B0
PTP
BYTE 1
801
MSG
MSG
MSG
BYTE 0
802
I/O RAM SRC
IO RAM (SRC NODE)
TX
TX EVENT
BRIDGE
813
814
812
811
EVENT
DATA B4
DATA B3
DATA B1
DATA B0
CHAN
PTP
TAIL
A PACKET TRANSFERING ONE WORD OF DATA TO A SINGLE DESTINATION
POINT-TO-POINT HEADER
BRIDGE
RX EVENT
RX
IO RAM (DST NODE)
I/O RAM DST
817
DST ADDR + 4
DST ADDR
815
DATA B3
DATA B2
DATA B1
DATA B0
BYTE 3
BYTE 2
BYTE 1
BYTE 0

FIG. 8

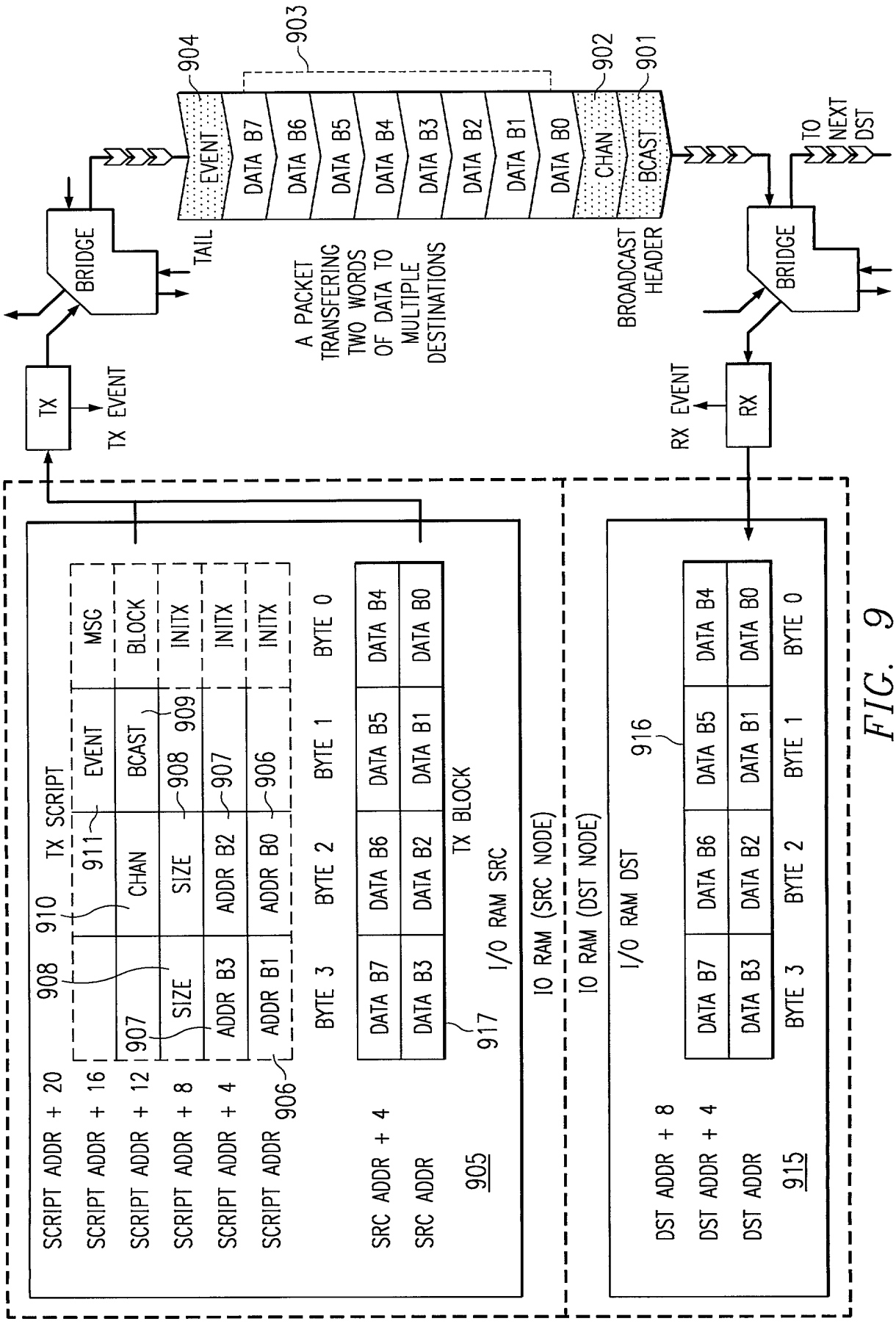

903
904
902
901
EVENT
DATA B7
DATA B6
DATA B5
DATA B4
DATA B3
DATA B2
DATA B1
DATA B0
CHAN
BCAST
TAIL
BROADCAST HEADER
A PACKET TRANSFERING TWO WORDS OF DATA TO MULTIPLE DESTINATIONS
TO NEXT DST
BRIDGE
BRIDGE
TX
TX EVENT
RX
RX EVENT
SCRIPT ADDR + 20
SCRIPT ADDR + 16
SCRIPT ADDR + 12
SCRIPT ADDR + 8
SCRIPT ADDR + 4
SCRIPT ADDR
906
907
908
910
911
TX SCRIPT
EVENT
CHAN
BCAST
SIZE
ADDR B2
ADDR B0
MSG
BLOCK
INITX
INITX
INITX
909
BYTE 3
BYTE 2
BYTE 1
BYTE 0
SRC ADDR + 4
SRC ADDR
905
DATA B7
DATA B3
DATA B6
DATA B2
DATA B5
DATA B1
DATA B4
DATA B0
TX BLOCK
917
I/O RAM SRC
IO RAM (SRC NODE)
IO RAM (DST NODE)
I/O RAM DST
916
DST ADDR + 8
DST ADDR + 4
DST ADDR
915
DATA B7
DATA B3
DATA B6
DATA B2
DATA B5
DATA B1
DATA B4
DATA B0
BYTE 3
BYTE 2
BYTE 1
BYTE 0

FIG. 9

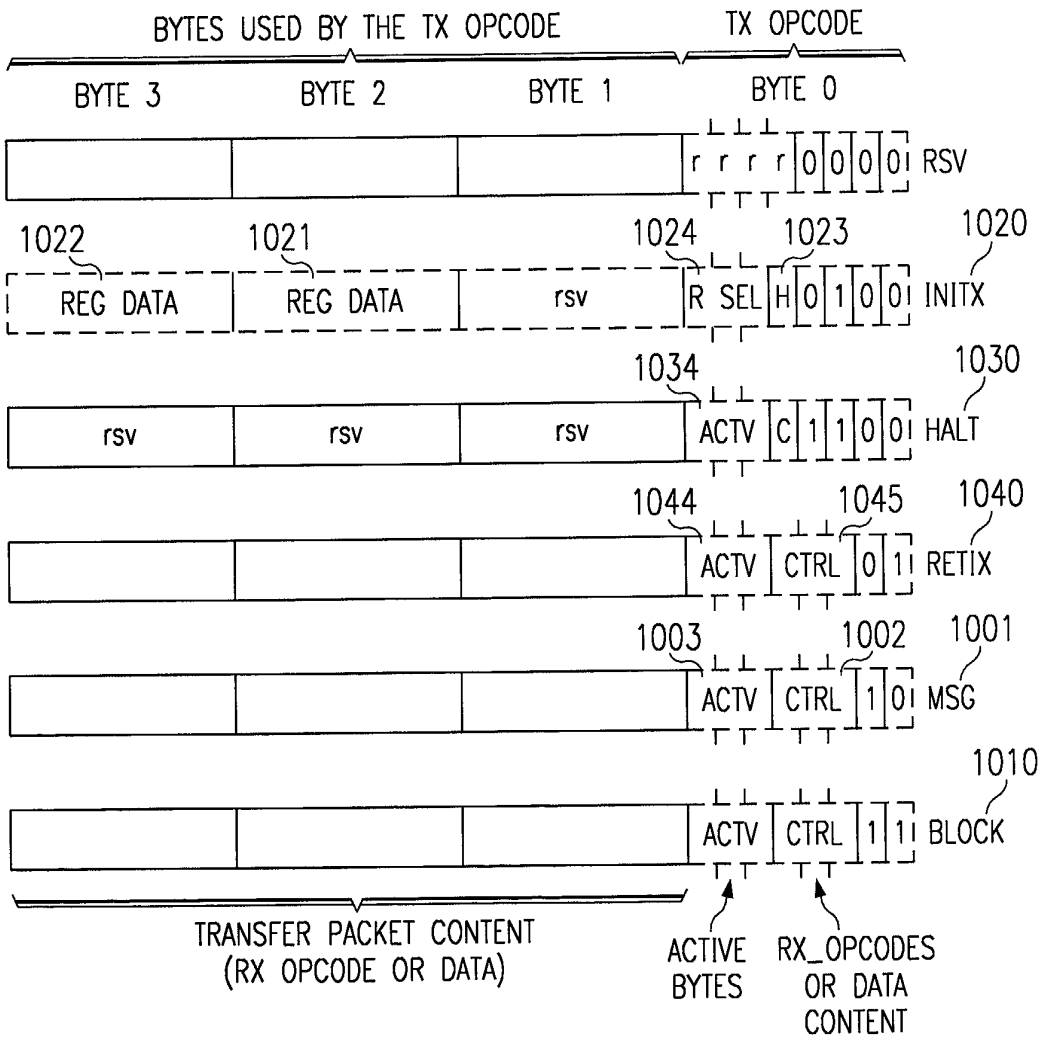


FIG. 10

RESERVED FOR FUTURE USE

INITIALIZE TRANSMITTER REGISTER(S)

HALT EXECUTION OF BATCH OPCODES

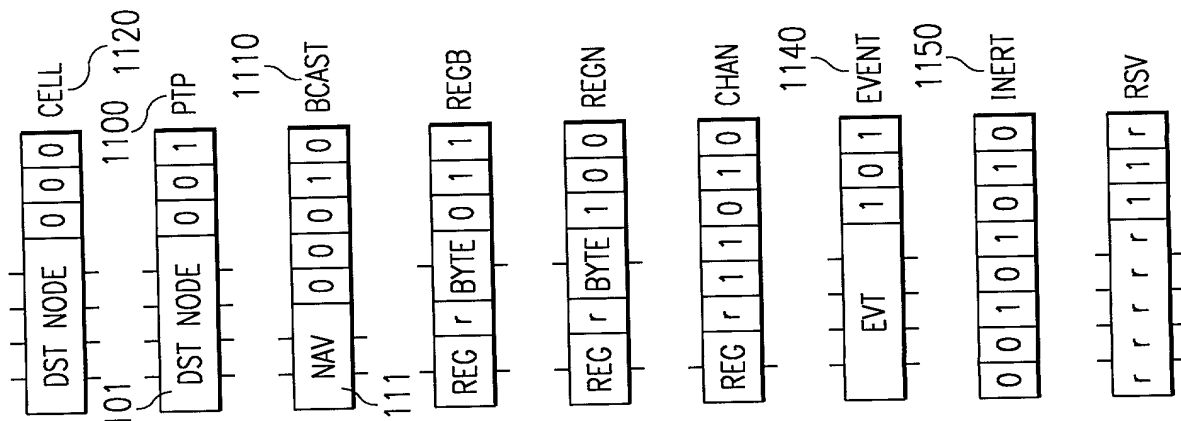
RETURN FROM INTERRUPT SCRIPT TO BATCH SCRIPT

TRANSMIT DATA/RX_OPCODES EMBEDDED IN TX OPCODE

TRANSMIT A DATA BLOCK LOCATED ELSEWHERE IN I/O RAM

r = RESERVED

FIG. 11



NAVIGATE THE PACKET ACROSS ONE COMMUNICATIONS CELL ON THE WAY TO ANOTHER CELL

NAVIGATE THE PACKET TO ONE OF 32 DSP NODES WITHIN A LOCAL COMMUNICATION CELL

NAVIGATE A SINGLE PACKET AND DELIVER SAME DATA INTO UP TO 32 NODES WITHIN A LOCAL COMMUNICATIONS CELL

LOAD A SINGLE BYTE (IMMEDIATELY FOLLOWING THIS OPCODE) INTO ONE OF THE 3 BRIDGE CONFIGURATION REGISTERS

LOAD A SINGLE BYTE (IMMEDIATELY FOLLOWING THIS OPCODE) INTO ONE OF 4 RECEIVER ADDRESS REGISTERS. SAME CHANNEL IS SELECTED AS AN ACTIVE CHANNEL TO RECEIVE DATA

SELECT ONE OF 4 RECEIVER ADDRESS REGISTERS AS AN ACTIVE CHANNEL TO RECEIVE DATA

USED TO SIGNAL TRANSMITTER EVENTS WHEN DATA IS LEAVING THE SOURCE NODE AND RECEIVER EVENTS WHEN DATA IS WRITTEN TO IO MEMORY OF THE DESTINATION NODE

USED BY THE TRANSMITTER FOR PADDING PACKET TAILS WHEN CONVERTING 8-BIT INTERNAL STREAMS TO 16-BIT EXTERNAL DATA STREAMS

RESERVED FOR FUTURE USE

r = RESERVED

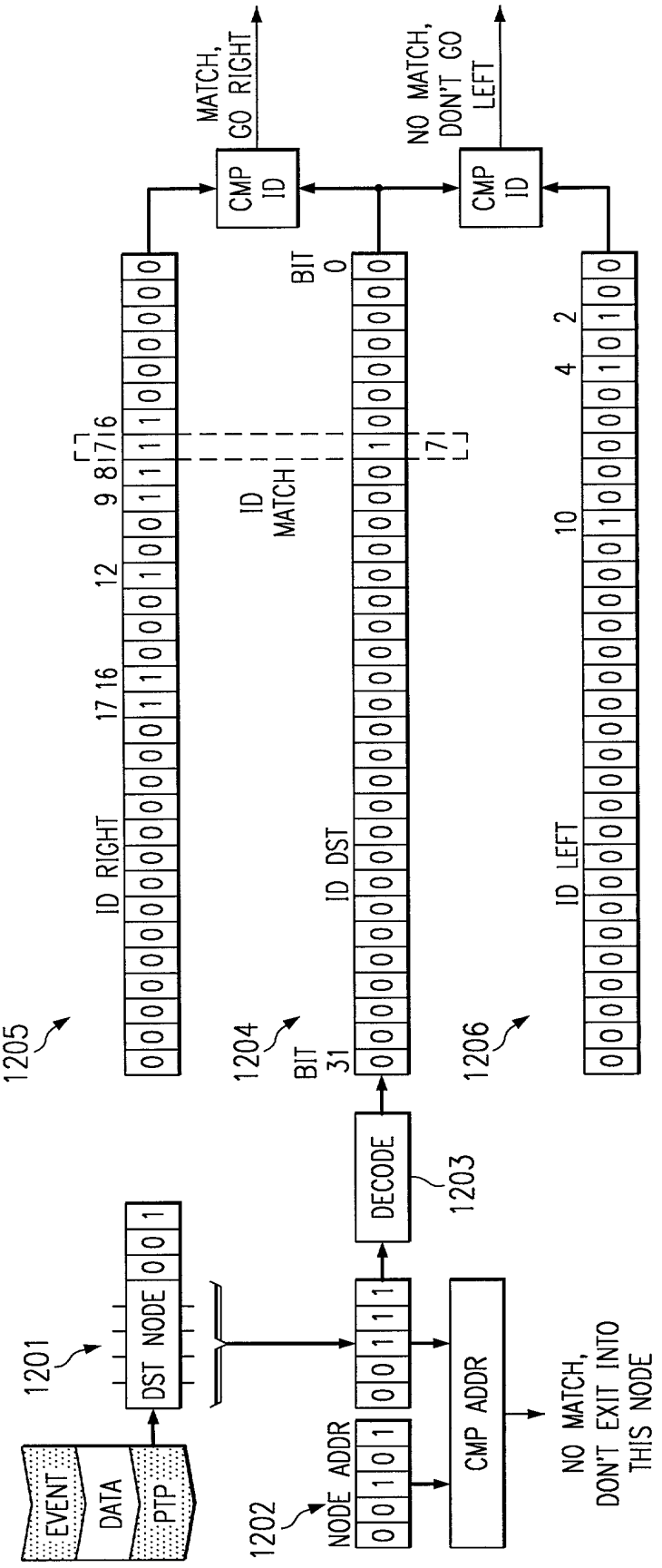

EVENT
DATA
PTP
1201
DST NODE
1202
NODE ADDR
CMP ADDR
NO MATCH,
DON'T EXIT INTO
THIS NODE
DECODE
1203
1204
BIT
31
ID DST
BIT
0
ID
MATCH
1205
ID RIGHT
1206
ID LEFT
CMP
ID
MATCH,
GO RIGHT
CMP
ID
NO MATCH,
DON'T GO
LEFT

FIG. 12

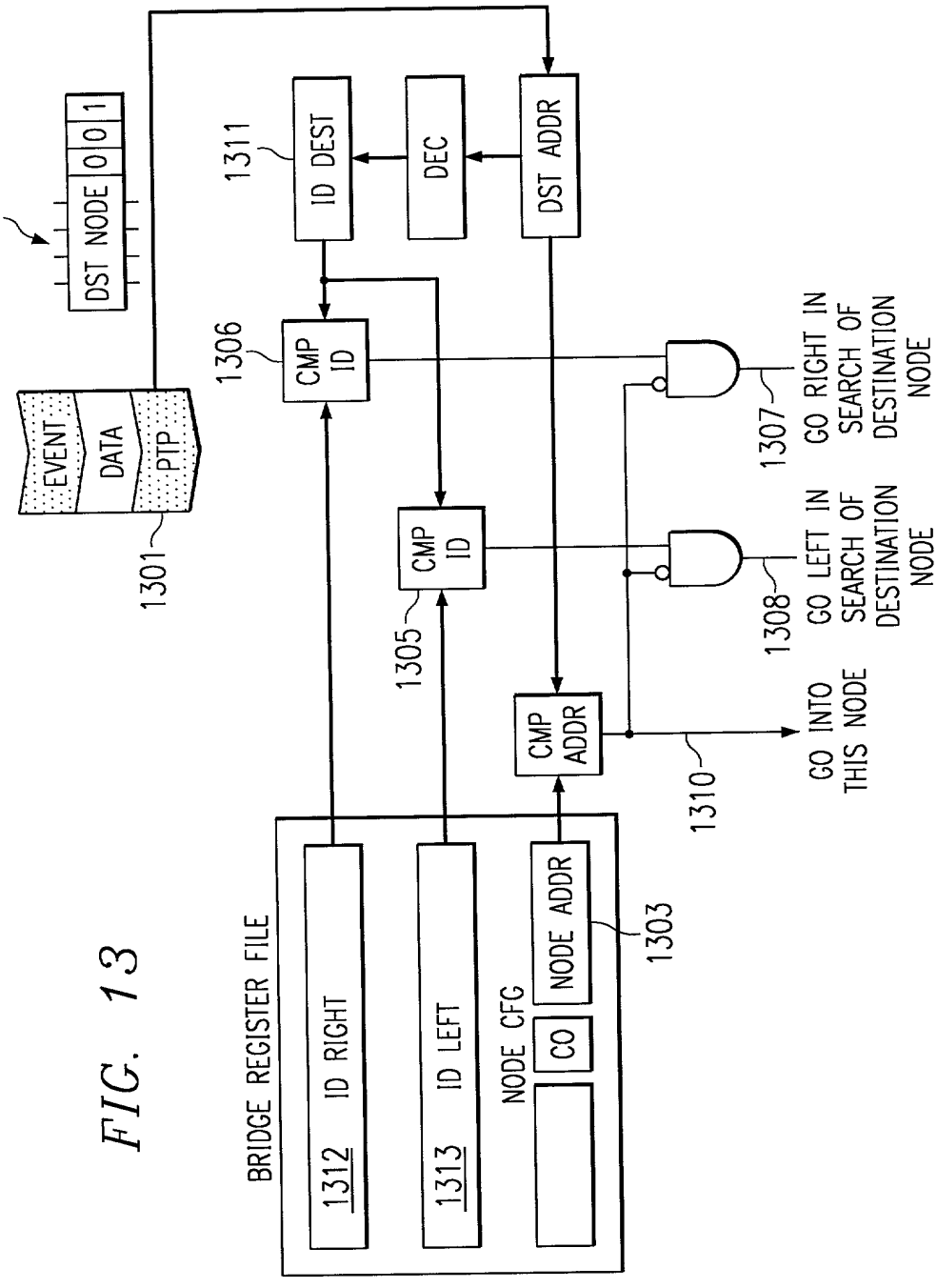

1302
DST NODE
0
0
1
1311
ID DEST
DEC
DST ADDR
EVENT
DATA
PTP
1301
1306
CMP ID
1305
CMP ID
CMP ADDR
1307
GO RIGHT IN SEARCH OF DESTINATION NODE
1308
GO LEFT IN SEARCH OF DESTINATION NODE
1310
GO INTO THIS NODE
BRIDGE REGISTER FILE
1312 ID RIGHT
1313 ID LEFT
NODE CFG
CO
NODE ADDR
1303

FIG. 13

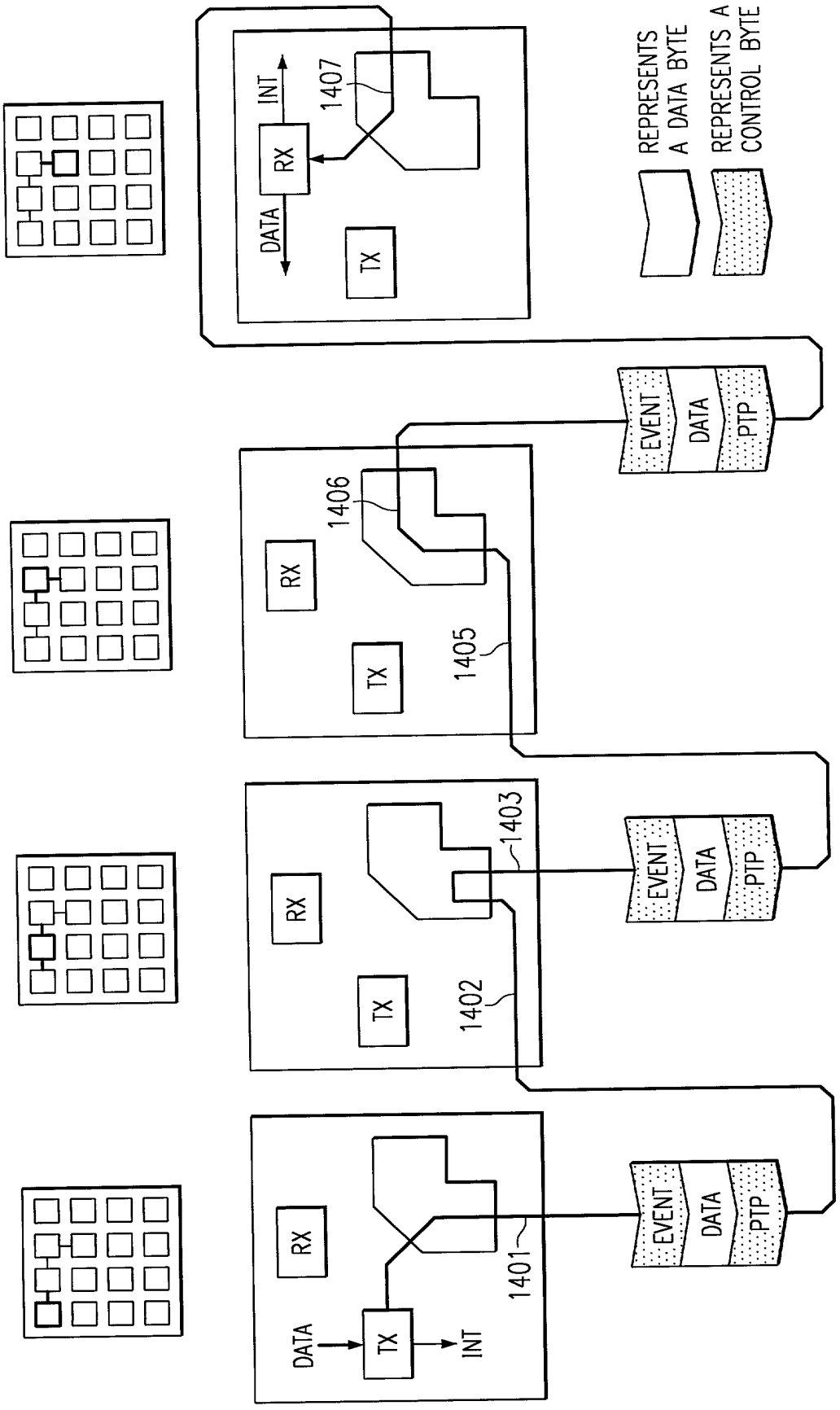

REPRESENTS A DATA BYTE
REPRESENTS A CONTROL BYTE
INT
1407
RX
DATA
TX
EVENT
DATA
PTP
1406
RX
TX
1405
1403
RX
TX
1402
1401
DATA
TX
INT

FIG. 14

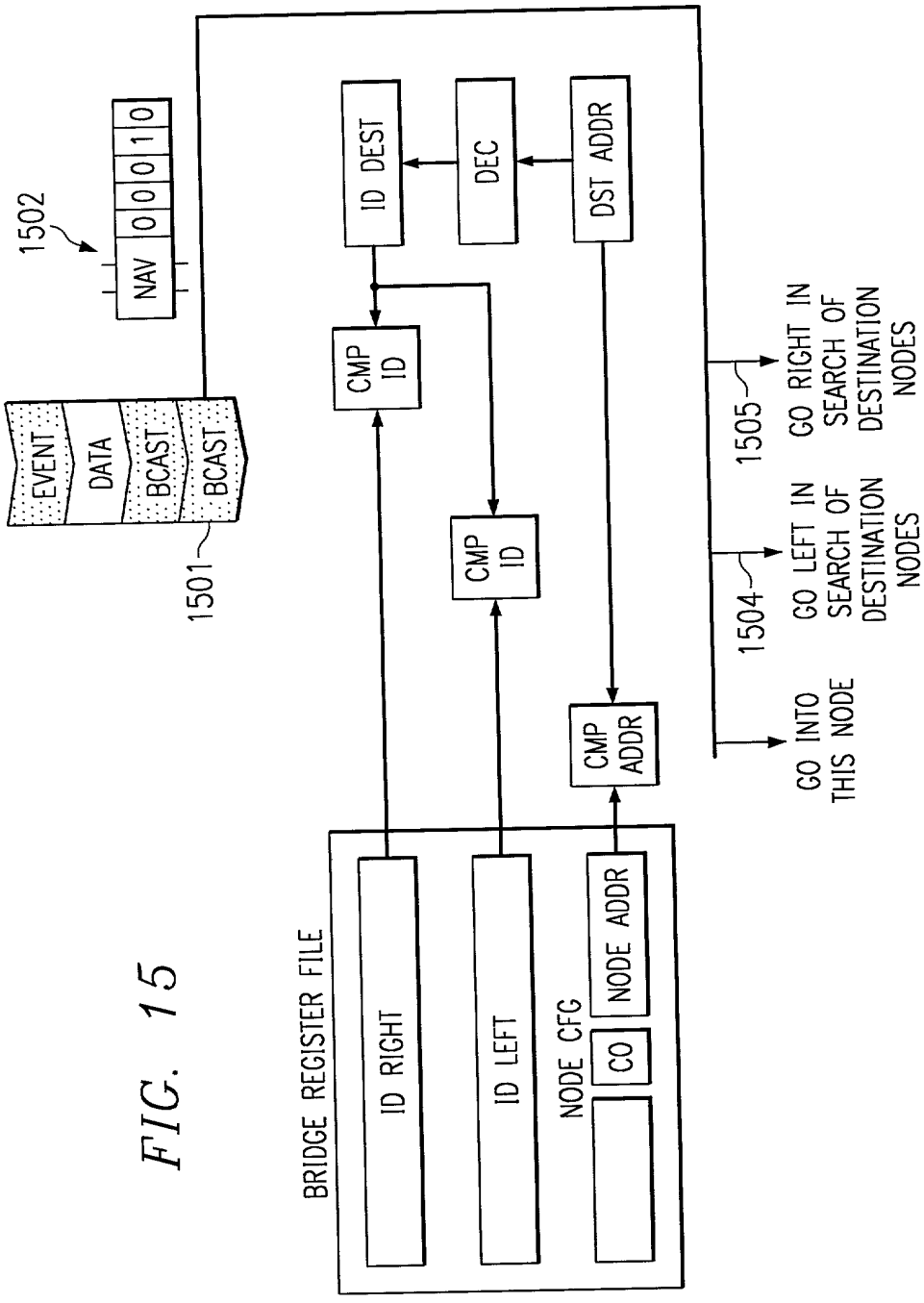

1502
NAV
0
0
0
1
0
EVENT
DATA
BCAST
BCAST
1501
ID DEST
DEC
DST ADDR
CMP ID
CMP ID
CMP ADDR
1505
GO RIGHT IN SEARCH OF DESTINATION NODES
1504
GO LEFT IN SEARCH OF DESTINATION NODES
GO INTO THIS NODE
BRIDGE REGISTER FILE
ID RIGHT
ID LEFT
NODE CFG
CO
NODE ADDR

FIG. 15

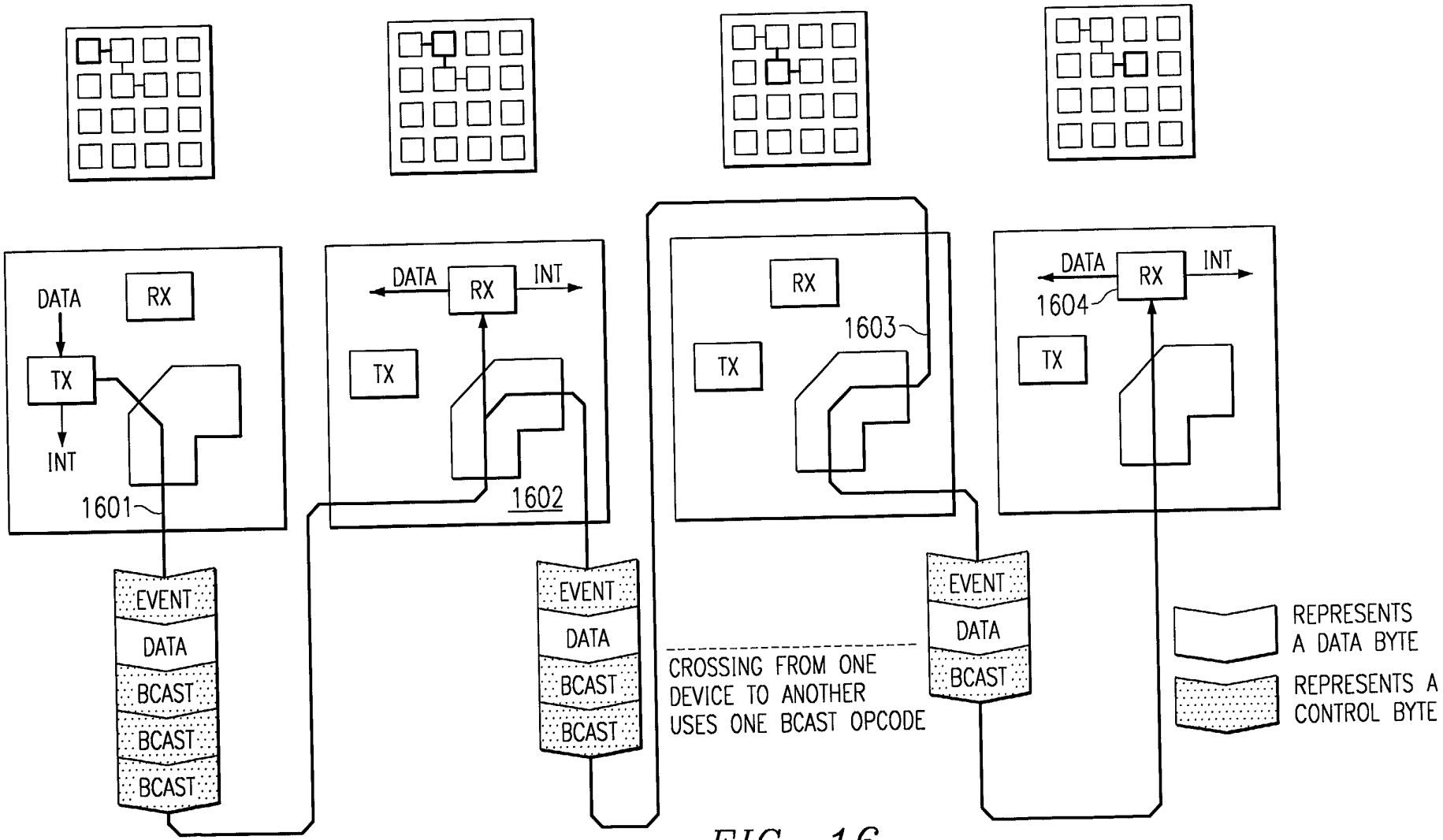

DATA
RX
TX
INT
1601
DATA
RX
INT
TX
1602
RX
1603
TX
DATA
RX
INT
1604
TX
EVENT
DATA
BCAST
BCAST
BCAST
EVENT
DATA
BCAST
BCAST
CROSSING FROM ONE
DEVICE TO ANOTHER
USES ONE BCAST OPCODE
EVENT
DATA
BCAST
REPRESENTS
A DATA BYTE
REPRESENTS A
CONTROL BYTE

FIG. 16

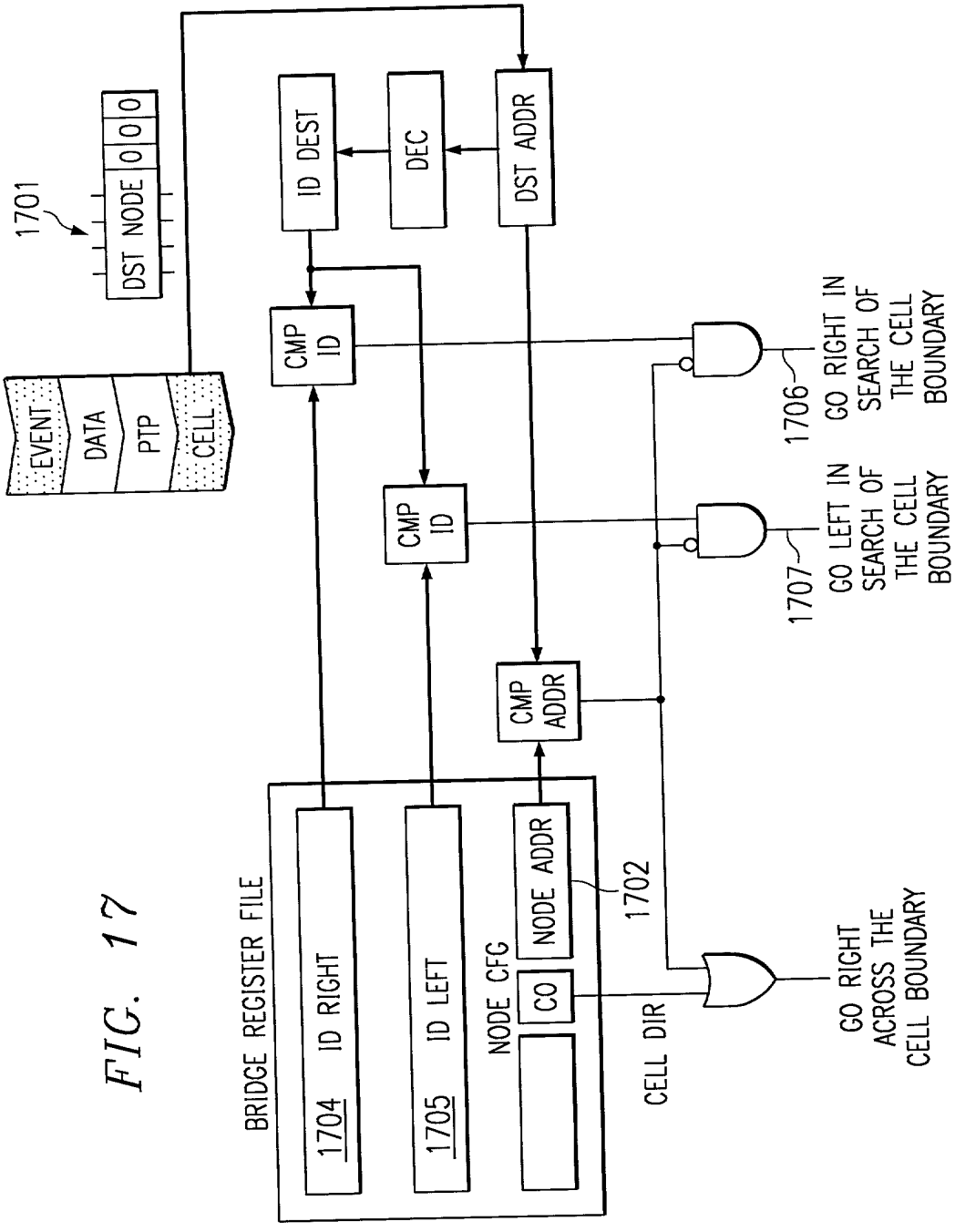

1701
DST NODE
0
0
0
EVENT
DATA
PTP
CELL
ID DEST
DEC
DST ADDR
CMP ID
CMP ID
CMP ADDR
1706
GO RIGHT IN SEARCH OF THE CELL BOUNDARY
1707
GO LEFT IN SEARCH OF THE CELL BOUNDARY
BRIDGE REGISTER FILE
1704 ID RIGHT
1705 ID LEFT
NODE CFG
CO
NODE ADDR
1702
CELL DIR
GO RIGHT ACROSS THE CELL BOUNDARY

FIG. 17

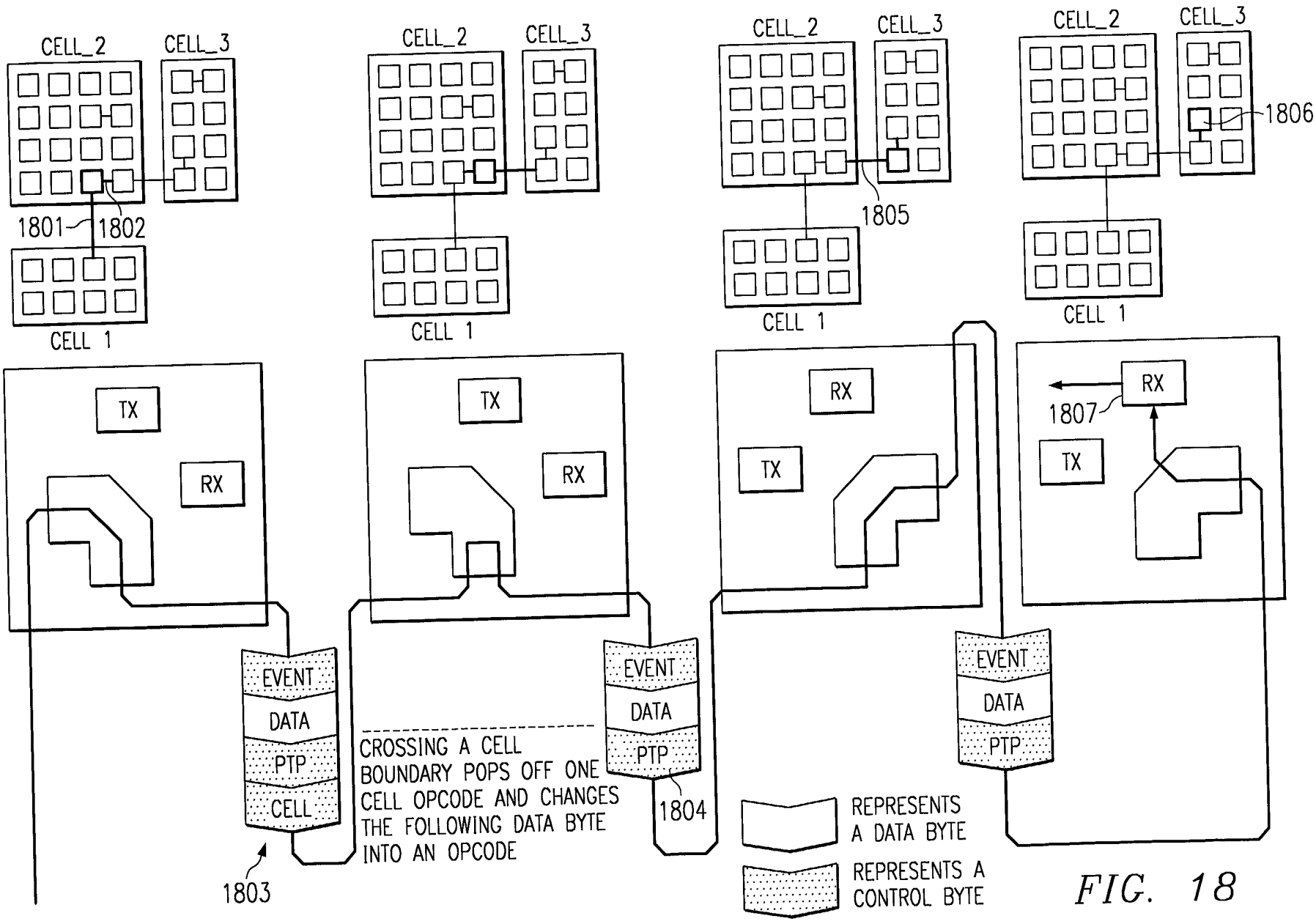

CELL_2
CELL_3
1801
1802
CELL 1
TX
RX
EVENT
DATA
PTP
CELL
1803
CROSSING A CELL BOUNDARY POPS OFF ONE CELL OPCODE AND CHANGES THE FOLLOWING DATA BYTE INTO AN OPCODE
1804
1805
1806
1807
REPRESENTS A DATA BYTE
REPRESENTS A CONTROL BYTE

FIG. 18

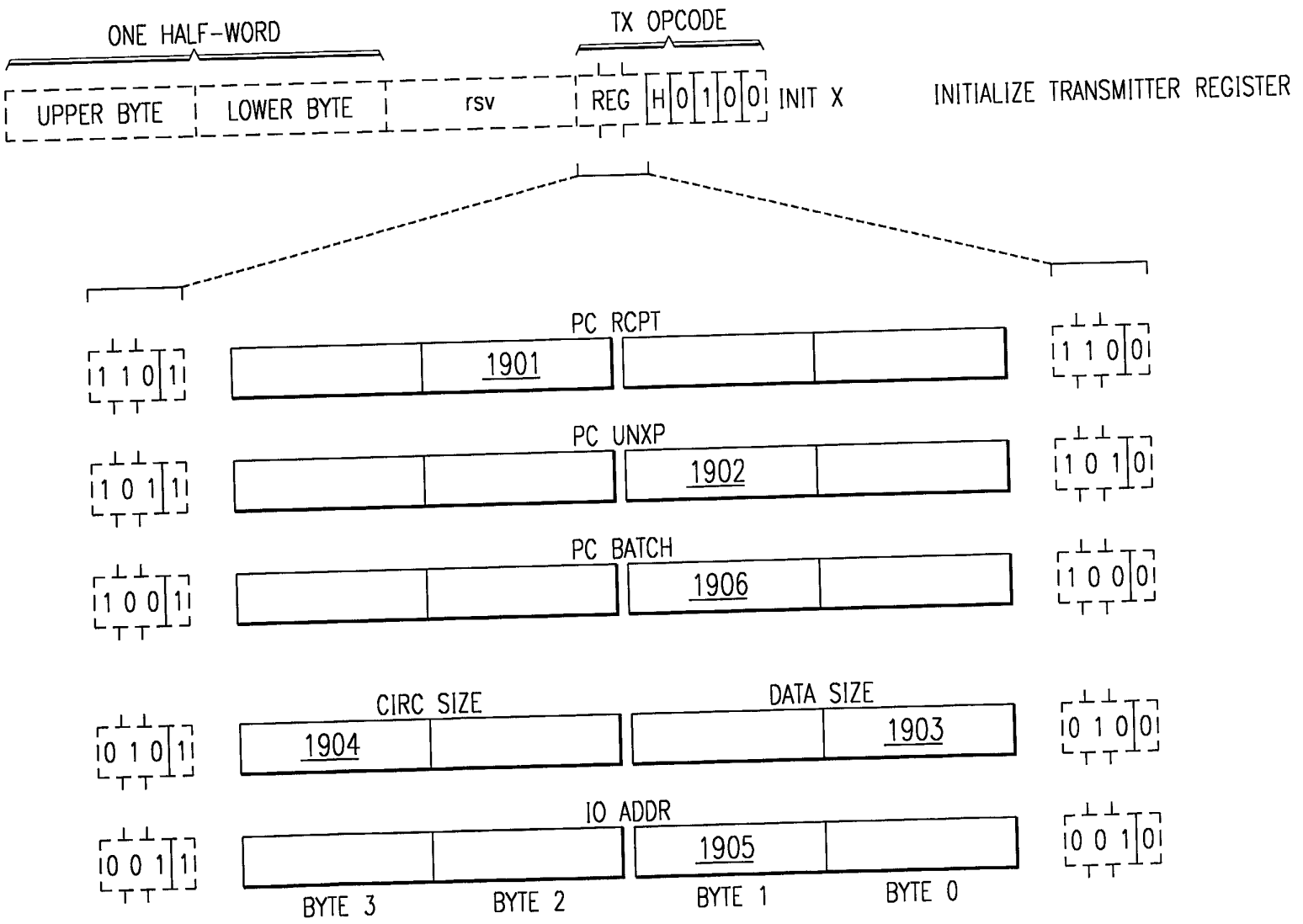

ONE HALF-WORD
TX OPCODE
UPPER BYTE
LOWER BYTE
rsv
REG
H 0 1 0 0
INIT X
INITIALIZE TRANSMITTER REGISTER
PC RCPT
1901
1 1 0 1
1 1 0 0
PC UNXP
1902
1 0 1 1
1 0 1 0
PC BATCH
1906
1 0 0 1
1 0 0 0
CIRC SIZE
1904
DATA SIZE
1903
0 1 0 1
0 1 0 0
IO ADDR
1905
0 0 1 1
0 0 1 0
BYTE 3
BYTE 2
BYTE 1
BYTE 0

FIG. 19

FIG. 20

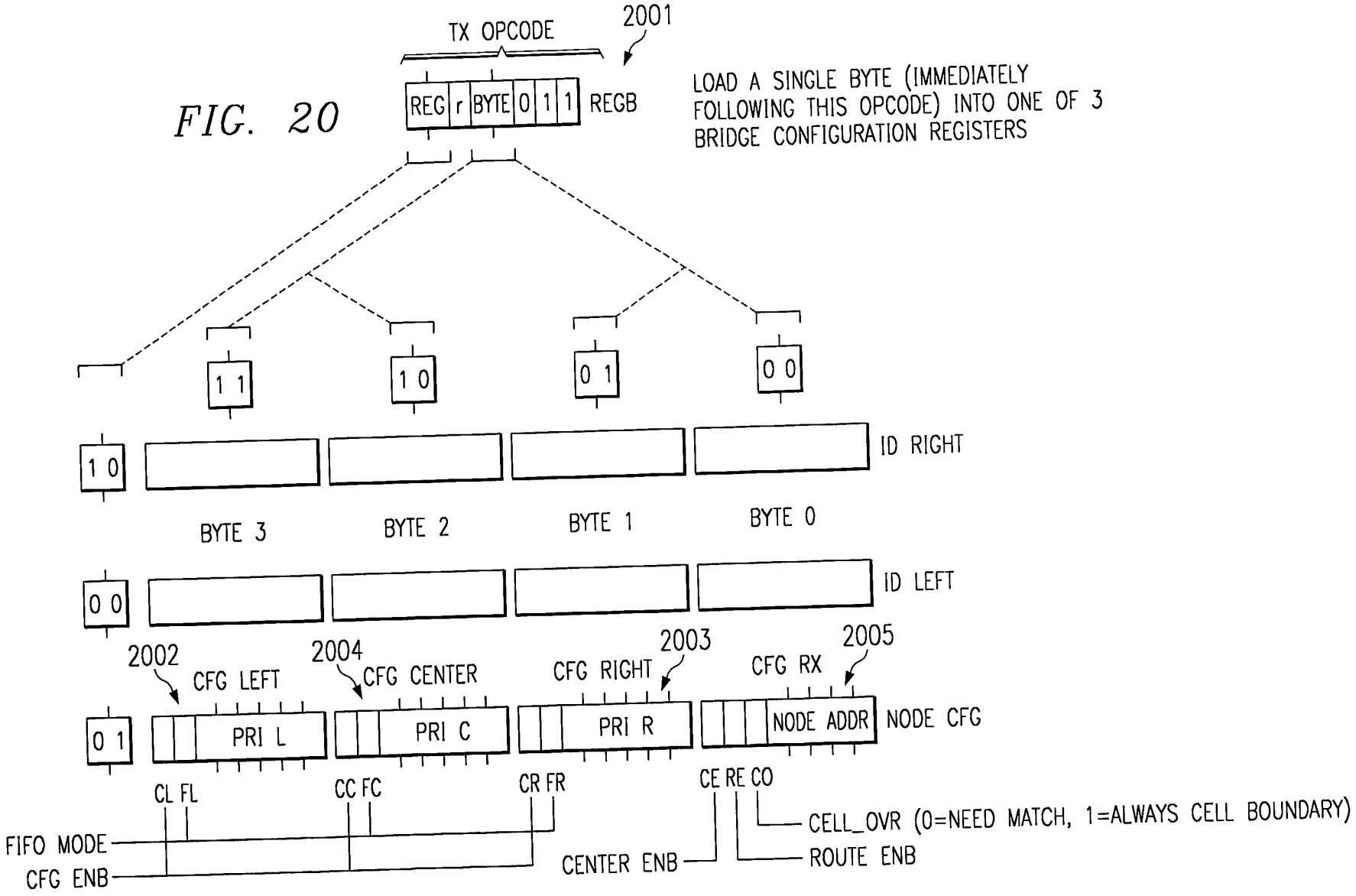
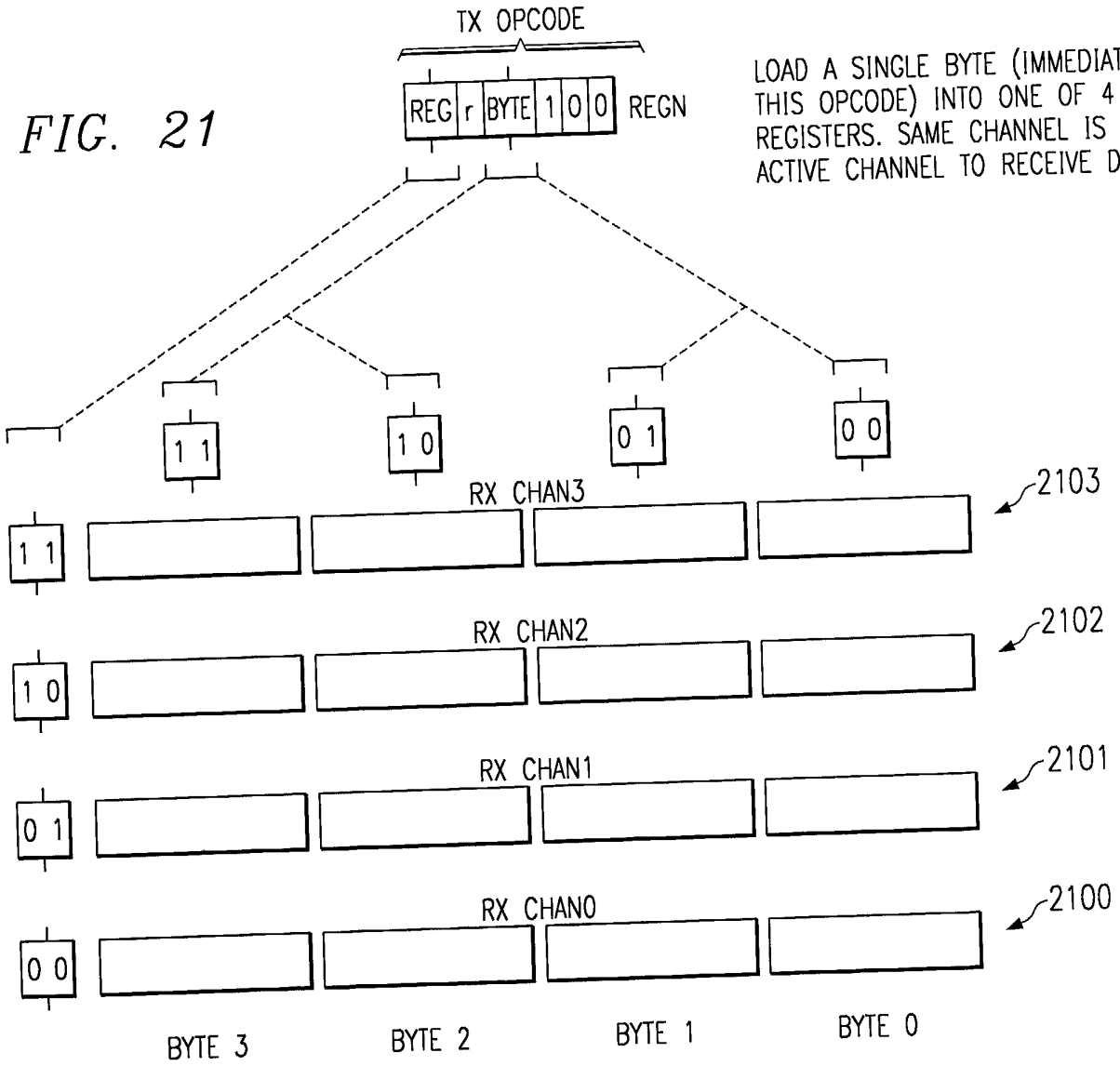

TX OPCODE
2001
REG r BYTE 0 1 1 REGB
LOAD A SINGLE BYTE (IMMEDIATELY FOLLOWING THIS OPCODE) INTO ONE OF 3 BRIDGE CONFIGURATION REGISTERS
1 1
1 0
0 1
0 0
1 0
ID RIGHT
BYTE 3
BYTE 2
BYTE 1
BYTE 0
0 0
ID LEFT
2002
CFG LEFT
2004
CFG CENTER
CFG RIGHT
2003
CFG RX
2005
0 1
PRI L
PRI C
PRI R
NODE ADDR
NODE CFG
CL FL
CC FC
CR FR
CE RE CO
CELL_OVR (0=NEED MATCH, 1=ALWAYS CELL BOUNDARY)
FIFO MODE
CFG ENB
CENTER ENB
ROUTE ENB

FIG. 21


TX OPCODE
REG r BYTE 1 0 0 REGN
LOAD A SINGLE BYTE (IMMEDIATELY FOLLOWING THIS OPCODE) INTO ONE OF 4 RECEIVER CHANNEL REGISTERS. SAME CHANNEL IS SELECTED AS AN ACTIVE CHANNEL TO RECEIVE DATA
1 1
1 0
0 1
0 0
RX CHAN3
2103
RX CHAN2
2102
RX CHAN1
2101
RX CHAN0
2100
BYTE 3
BYTE 2
BYTE 1
BYTE 0

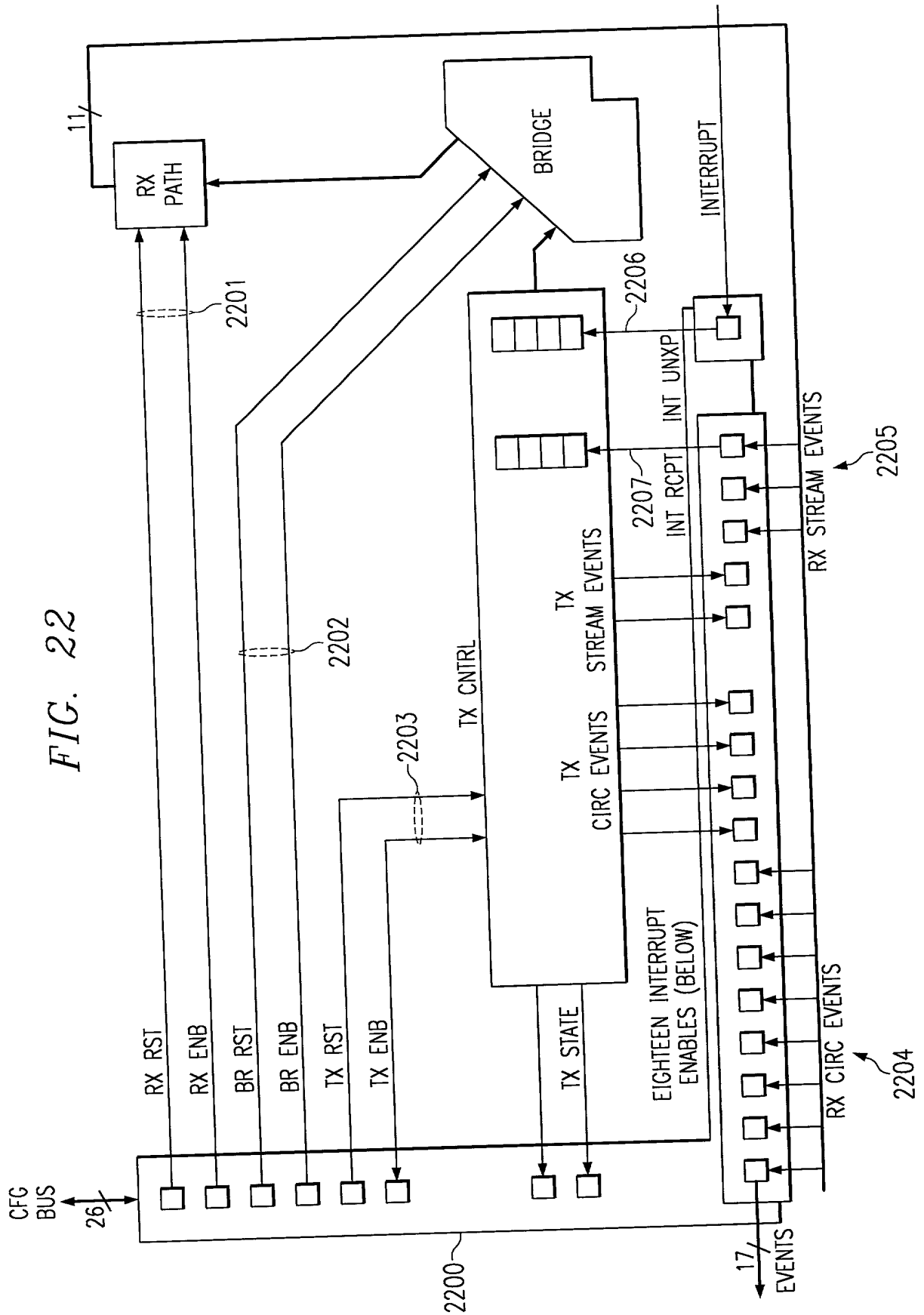

11
RX PATH
BRIDGE
INTERRUPT
2201
2206
2202
2207
INT RCPT
INT UNXP
2205
RX STREAM EVENTS
TX STREAM EVENTS
2203
TX CNTRL
TX CIRC EVENTS
RX RST
RX ENB
BR RST
BR ENB
TX RST
TX ENB
TX STATE
EIGHTEEN INTERRUPT ENABLES (BELOW)
RX CIRC EVENTS
2204
CFG BUS
26
2200
17
EVENTS

FIG. 22

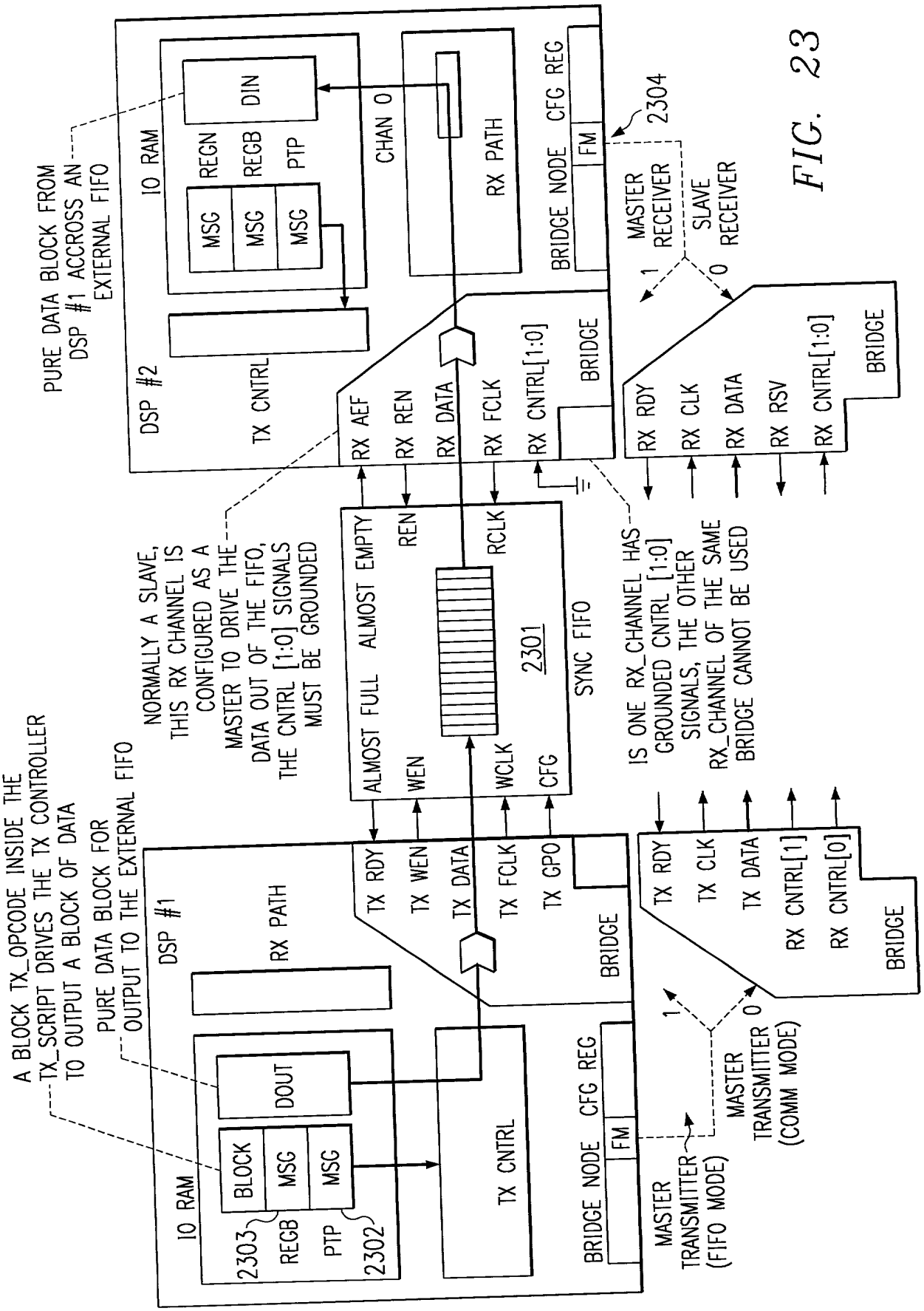

A BLOCK TX_OPCODE INSIDE THE TX_SCRIPT DRIVES THE TX CONTROLLER TO OUTPUT A BLOCK OF DATA
PURE DATA BLOCK FOR OUTPUT TO THE EXTERNAL FIFO
NORMALLY A SLAVE, THIS RX CHANNEL IS CONFIGURED AS A MASTER TO DRIVE THE DATA OUT OF THE FIFO, THE CNTRL [1:0] SIGNALS MUST BE GROUNDED
IS ONE RX_CHANNEL HAS GROUNDED CNTRL [1:0] SIGNALS, THE OTHER RX_CHANNEL OF THE SAME BRIDGE CANNOT BE USED
PURE DATA BLOCK FROM DSP #1 ACCROSS AN EXTERNAL FIFO
DSP #1
IO RAM
BLOCK
MSG
MSG
DOUT
REGB
PTP
2303
2302
RX PATH
TX CNTRL
BRIDGE NODE CFG REG
FM
MASTER TRANSMITTER (FIFO MODE)
MASTER TRANSMITTER (COMM MODE)
TX RDY
TX WEN
TX DATA
TX FCLK
TX GPO
BRIDGE
TX CLK
RX CNTRL[1]
RX CNTRL[0]
ALMOST FULL
ALMOST EMPTY
REN
WEN
RCLK
WCLK
CFG
2301
SYNC FIFO
DSP #2
TX CNTRL
IO RAM
MSG
MSG
MSG
REGN
REGB
PTP
DIN
CHAN 0
RX PATH
BRIDGE NODE CFG REG
FM
2304
MASTER RECEIVER
SLAVE RECEIVER
RX AEF
RX REN
RX DATA
RX FCLK
RX CNTRL[1:0]
BRIDGE
RX RDY
RX CLK
RX DATA
RX RSV
RX CNTRL[1:0]
BRIDGE

FIG. 23

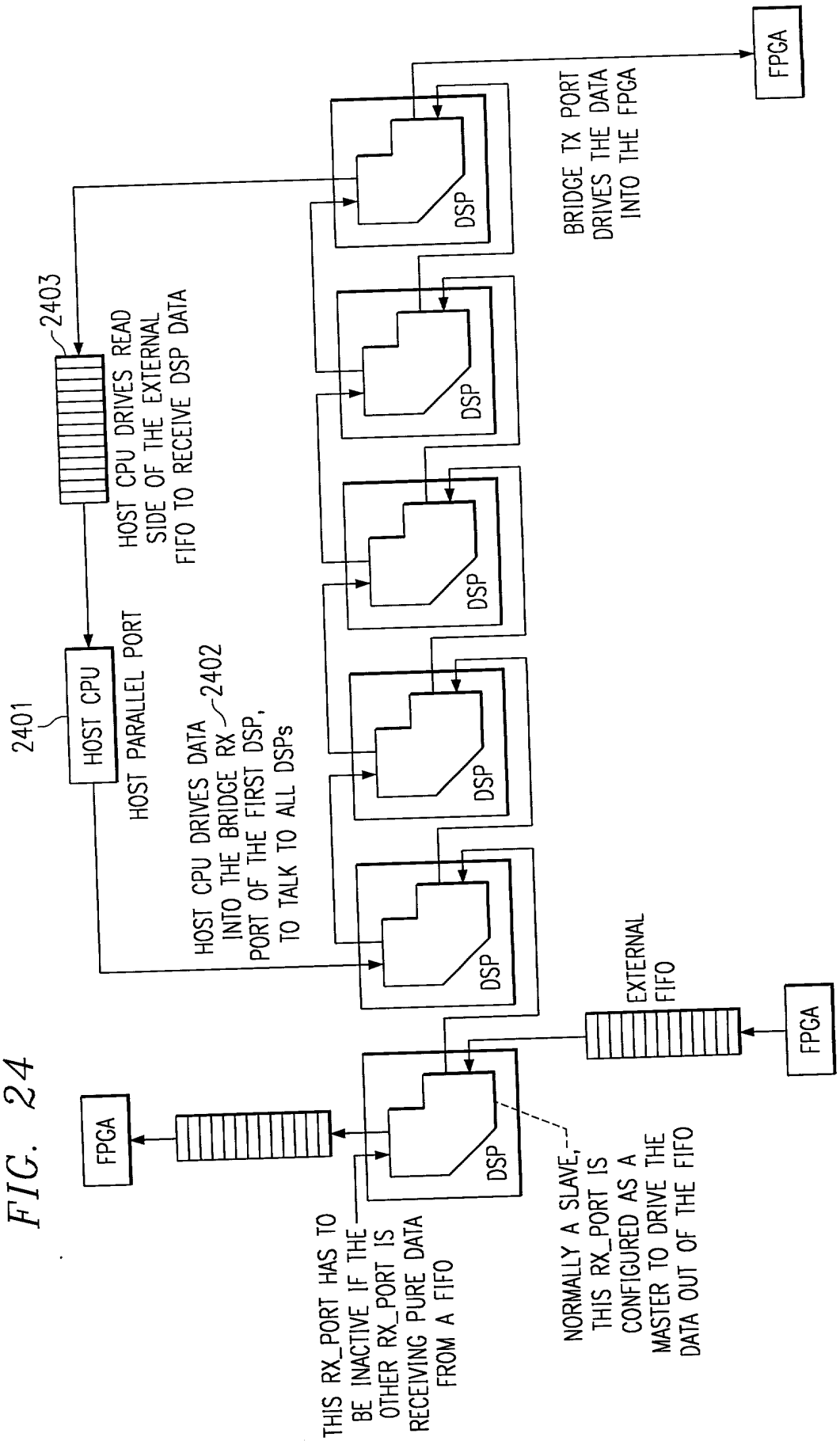

2401
HOST CPU
HOST PARALLEL PORT
2402
HOST CPU DRIVES DATA INTO THE BRIDGE RX PORT OF THE FIRST DSP, TO TALK TO ALL DSPs
2403
HOST CPU DRIVES READ SIDE OF THE EXTERNAL FIFO TO RECEIVE DSP DATA
DSP
BRIDGE TX PORT DRIVES THE DATA INTO THE FPGA
FPGA
EXTERNAL FIFO
FPGA
THIS RX_PORT HAS TO BE INACTIVE IF THE OTHER RX_PORT IS RECEIVING PURE DATA FROM A FIFO
NORMALLY A SLAVE, THIS RX_PORT IS CONFIGURED AS A MASTER TO DRIVE THE DATA OUT OF THE FIFO

FIG. 24

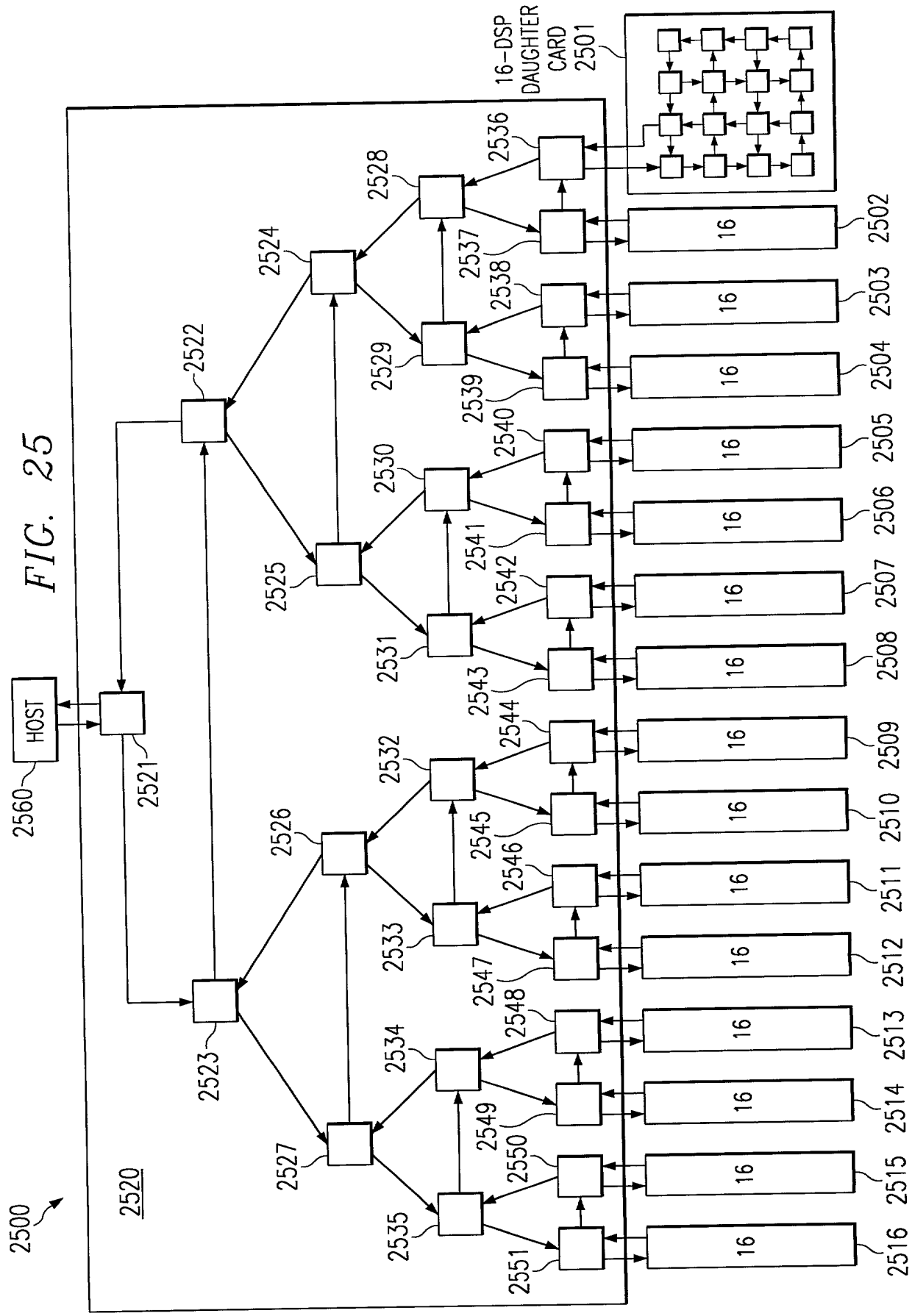

2500
2520
HOST
2560
2521
2522
2523
2524
2525
2526
2527
2528
2529
2530
2531
2532
2533
2534
2535
2536
2537
2538
2539
2540
2541
2542
2543
2544
2545
2546
2547
2548
2549
2550
2551
16-DSP DAUGHTER CARD 2501
16
2502
2503
2504
2505
2506
2507
2508
2509
2510
2511
2512
2513
2514
2515
2516

FIG. 25